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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,048	06/19/2003	Louis A. Lippincott		6019

7590 07/05/2007

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EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
07/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/600,048	LIPPINCOTT, LOUIS A.	
	Examiner	Art Unit	
	Hau H. Nguyen	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *9,11,16,20 and 26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10,12-15,17-19,21-25 and 27-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The response filed on April 16, 2007 has been carefully considered in preparing for this Office Action.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-8, 10, 12, 18, 19, 21-25, 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tulpule et al. (U.S. Patent No. 4,933,836, Tulpule, hereinafter) in view of Galicki et al. (U.S. Patent No. 6,967,950, hereinafter, Galicki).

As per claim 1, Tulpule teach an apparatus comprising:

a first processor 12 (Fig. 1) having two or more processor elements (Fig. 7, col. 13, ll. 32-48), and two or more input/output ports coupled together by a first port ring this is within the first processor (Fig. 2, col. 8, ll. 34-40); and

a second processor 18, which is similar to the first processor 12, couples to the first processor 12 through at least one I/O port of a third port ring within a third processor 14 (Fig. 1).

Tulpule fails to teach the two or more I/O ports in the first processor, the second processor and the third processor are configured to establish a logical connection between the first processor and the second processor, the logical connection to originate at first processor and to traverse through the third processor and to complete at the second processor, wherein the logical connection is established based on other active logical connections that include at least

one of the first processor, the second processor and third processor. However, this is what Galicki teaches. As shown in Fig. 2, Galicki teach an array of multiple processors that are configured to establish a logical connection between the first processor (e.g. DSP #1) and the second processor (e.g. DSP #7) (col. 4, lines 21-44), wherein the logical originate at the first processor DSP #1 and to traverse through the third processor (e.g. DSP # 2) and to complete at the second processor DSP #7, wherein the logical connection is established based on other active logical connections (*i.e. based on other active receive channels as shown in Figs. 7-9*) that include at least one of the first processor, the second processor, and the third processor (col. 8, lines 48-56). (It is also noted that Galicki teaches *broadcast packets can navigate to multiple destinations* (col. 5, lines 48-62); i.e., more than one logical connections are established between the processors).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Galicki in combination with the method as taught by Tulpule in order to increase system performance, simplifying software and decreasing central processing unit/direct memory access loading (col. 10, lines 55-67).

As per claim 2, as shown in Fig. 1, Tulpule, teach the two or more I/O ports of the first processor is not directly connected to the two or more I/O ports of the second processor.

As per claims 3, Tulpule fails to teach the first, second, and third processors are part of a number of processors in a point-to-point configuration. However, Galicki et al. teach a method of transferring data between multiple digital signal processors from the source processor 201 to the destination processor in a point-to-point configuration (Fig. 2, col. 4, ll. 45-55).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Galicki in combination with the method as taught by Tulpule in order to increase system performance, simplifies software and decreases central processing unit and direct memory access unit loading (col. 3, ll. 10-20).

As per claim 4, although Tulpule does not explicitly teach the first processor transmitting output from an image process operation to the second processor, Tulpule does teach the processors are the signal processors, and also suggest using for image processing (col. 1, ll. 61-68). Although Tulpule fails to teach transmitting of image data to the second processor from the first processor based on a logical connection, Galicki teaches this feature as cited above (implemented via the datapipe).

As per claim 5, although Tulpule fails to explicitly teach the I/O ports of the processors comprising a FIFO memory, Tulpule does teach at the I/O ports of the signal processor 12 (such as "North" and "South" ports, Fig. 3) comprising a dual port RAM 74 and 76 to communicate with other modular entities (col. 10, ll. 36-41). Therefore, it would have been obvious to one skilled in the art to modify the memories 74 and 76 into FIFO in order to queue the commands received or transmitted at each processor.

As per claim 6, Tulpule does not explicitly teach the I/O ports of each processor comprising a transmitter port and receiver port, wherein the first processor configured to transmit the output based a handshake protocol among the receiver ports and the transmitter ports of the first processor, the second processor, and the third processor. However, this is taught by Galicki with reference to Figs. 10 and 11.

As per claim 7, as cited above, the teachings of Tulpule and Galicki in combination teach the limitations of claim 7. Specifically, Tulpule teach a plurality of signal processors 12-18, each includes plurality of I/O ports configured in a port ring, at least one signal processor 24, which may be used in image processing, wherein one signal processor coupled to another signal processor via the I/O ports of the port rings. Galicki teach the digital signal processors are coupled together in a point-to-point configuration. With reference to claim 1, Galick teach the number of ports within the port rings of the number of image signal processors are configured to establish logical connections between the number of image signal processors, wherein the logical connections are to originate at a source image signal processor (DSP#1) of the number of image signal processors and to traverse a number of intermediate image signal processors (DSP#2, DSP#3) of the number of image signal processors and to complete at a destination image signal processor (DSP#7) of the number of image signal processors, wherein the source image signal processor is to transmit an initialize signal (included in the packet header, col. 7, lines 30-35, and col. 6, lines 43-55), prior to transmission of data along the logical connection, through the number of intermediate image signal processors to the destination image signal processor in the order that data is transmitted in the logical connection.

As per claim 8, as cited above, the combined system teaches the at least one processor element in a first of the number of image processors is configured to perform one of a number of image processed-based operations.

Claims 10 and 12, which are similar to claims 4 and 5, are thus rejected under the same rationale.

As per claim 18, the limitations of which have been addressed above with reference to claims 1 and 7, further requires registering a logical connection with a number of ports of port rings of a number of image signal processors in a logical connection based on transmission of an initialization signal through a logical connection. However, this is also taught by Galicki as cited above, wherein the header packet is examined at the I/O port of each DSP (col. 6, lines 43-55).

Claims 19, 21-25, 27-30, which are similar in scope to claims 6-10, 12, and 18 above, are rejected under similar rationale.

4. Claims 13-15, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tulpule et al. (U.S. Patent No. 4,933,836) in view of Galicki et al. (U.S. Patent No. 6,967,950), and further in view of Hsieh et al. (U.S. Patent No. 6,757,019, hereinafter, Hsieh).

As per claim 13, the teachings of Tulpule and Galicki are given in previous paragraph of this Office action. However, the combined system fails to explicitly teach or suggest a CMOS sensor to capture image data. This is what Hsieh teaches. As shown in Figs. 3 and 4, Hsieh teaches an image processor including a plurality of image signals processors 40, having a plurality of expansion interfaces (DMA 50, Fig. 5) configured to receive the image data to captured by the CMOS sensor 22 (col. 5, ll. 1-14). Hsieh also teaches the host processor configure a number of logical connection among the number of image signal processors 40 (Figs. 2A-2C, col. 4, ll. 13-24).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Hseih in combination with the method as taught by Tulpule and Galicki because CMOS image sensor provides high speed video capturing and thus further increase the overall image processing performance. Therefore, at least claim 13 would have been obvious.

As per claim 14, the combined system provides at least one image signal processor comprises a hardware accelerator (such as signal processor, Tulpule, or PEs 40, of Hsieh) to execute image process operations.

As per claim 15, Hsieh teaches the image processor comprises a global bus (such as, bus connects the PEs as shown in Fig. 2C) coupled to the number of expansion interfaces and the number of image signal processors, independent of the point-to-point configuration among the number of image signal processors.

As per claim 17, Galicki teaches traversal through the number of ports of the port rings of the at least one intermediate image signal processor is independent of image process operations by processor elements within the at least one intermediate image signal processors (Fig. 2, col. 4 12, ll. 45-55).

Response to Arguments

5. Applicant's arguments with respect to claims 1-8, 10, 12-15, 17-19, 21, 25, 27 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments with respect to claims 22-24, 28-30 have been fully considered but they are not persuasive for the reasons incorporated in the rejections above.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794.

The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

H. Nguyen

6/20/2007

KEE M. TUNG
SUPERVISORY PATENT EXAMINER